Venkateshwarlu Yellaswamy Gudur

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Career Objective

Aspiring for a dynamic and challenging work environment that encourages continuous learning and stimulate professional and personal growth

Educational Qualifications

Degree	Name of College/ School	Year	CGPA/Percentage
Master of Technology (VLSI Design)	Shri Ramdeobaba College of Engineering and Management, Nagpur (An Autonomous College of RTM Nagpur University)	2014	9.5/10
Bachelor of Engineering (Electronics and Telecommunication)	Walchand Institute of Technology, Solapur	2012	81.11
HSC	Walchand College of Arts & Science, Solapur	2008	93.5
SSC	D.R. Shriram English Medium School, Solapur	2006	87.86
GATE	-	2013	GATE Score 475
GATE	-	2014	GATE Score 411

Academic Projects

- **M. Tech Project**
  Title- Architectural Optimization of DSP Application and its Implementation using Soft Core Processor

  Fixed-width multipliers and the compensation techniques used in designing them are studied. A fixed-width two's-complement multiplier which gives minimum mean square error is designed. The multiplier consumes less power for product of low frequency signals. The multiplier designed is used as a custom peripheral in the environment of Microblaze, a soft core processor. Regular FFT and real-valued FFT are computed using the Microblaze system.

- **Personal Projects**

  Title- Area Efficient Carry Select Adder

  Adders of large bit-width inputs and square-root carry select adder (CSLA) are studied. Modified square-root CSLA architecture, published in IEEE in February 2012, is implemented on Spartan 2 board. The same design is also implemented at MOSFET level using Tanner EDA tools.

  Title- High ISO Noise Reduction in Images

  High ISO noise in images is studied. High ISO noise reduction design, published in IEEE in March 2012, is implemented. The implemented design is applied on images captured at different rates and ISO.

  Title- Image Processing on FPGA

  Basic image processing operations are studied and are implemented in VHDL. Spartan 3 FPGA board is used. Operations like image negative, image thresh holding are performed. Histogram equalization, edge detection are implemented using Microblaze processor.

- **BE Project**

  Title- Neonatal Thermo-Controller

  Objective of the project is to design a microcontroller board and other circuits and use this board for controlling temperature of a new born baby. An ATMEGA microcontroller circuit is designed. An Op-Amp amplifier circuit and a pulse rate sensor circuit are designed. Using AVR studio C language program is written to monitor pulse rate and to monitor and control temperature of the baby. A demo model of the project is implemented.

Areas of Interest

Digital System Design, Image Processing, Embedded System Design

Software Skills

C Language, VHDL, Matlab and Verilog

Lab and Technical Experience

- Worked on VHDL programmes of various digital modules like multiplier, ALU, sequential circuits, combinational circuits, etc. and implemented them on FPGA boards
- Interfaced various IO modules to LPC 2148 microcontroller. Various modules like keypad, LCD, stepper motor, etc. are interfaced
- Hands on experience on 8051, ATMEGA16, LPC2148 microcontrollers
- Worked on 36 channels logic analyzer CDLogic SLA2100 and 36 channels pattern generator DigiPat SPG2100

Academic Achievements

- First in M. Tech I, II, III and IV semesters
- University topper in First Year of BE
- Secured position among top three in Second and Third Year of BE
- First in SBC reserved category in Pune Board in HSC examination, second in college in HSC examination and secured first position in college in MHT-CET 2008 examination with 180 out of 200 marks
- Secured first position in school in SSC examination

Co-Curricular and Extra-Curricular Activities

- Secured third prize in **Project Competition** for the project entitled **Area Efficient Carry Select Adder**, at Aayam-2014 at PIET, Nagpur
- Secured second prize in **Quiz Competition** at WITChar-2012 at WIT, Solapur
- Secured second prize in **C Contest** by TESA committee at WIT, Solapur in 2011
- Chief Editor of Telugu Section of college magazine, Witness-2012 of WIT, Solapur
- Class Representative from first year to third year of BE
- Active participant in social works carried by college

Personal Details

Name	Venkateshwarlu
Name of Father	Yellaswamy
Last Name	Gudur
Name of Mother	Rajamani
Permanent Address	Plot No 31, Adarsh Nagar, Old Kumbhari Naka, MIDC Road, Solapur 413006
Email-Id	gudurvenkatesh@gmail.com
Mobile No	8421209918
Date of Birth and Age	10/06/1990, 24 years
Sex	Male
Marital Status	Single
Nationality	Indian
Languages known	Telugu, English, Hindi, Marathi

Declaration

The above information given by me is true to the best of my knowledge and belief.

Date: 01/10/2014

Place: Hyderabad

Venkateshwarlu Y Gudur